CODE EXAMPLE 3-2 `diag-level` Variable Set to `min` *(Continued)*

```
@(#) Sun Ultra 5/10 UPA/PCI  3.9 P2.1  Version 9 created 1997/08/
05 16:24
    DMMU TSB Reg Test
    DMMU Tag Access Reg Test
    IMMU TSB Reg Test
    IMMU Tag Access Reg Test
All Basic Cache Tests
    Dcache RAM Test
    Icache RAM Test
Sabre MCU Control & Status Regs Init and Tests
    Init Sabre MCU Control & Status Regs
    Initializing SC registers in SabreIO
Memory Probe and Init
    Probe Memory
    INFO:    256MB Bank 0
    bank 2:  0MB
frequency = 301, refvalue = 146, no_of_banks = 1
INFO: MC0 = 0x00000000.80001192, MC1 = 0x00000000.0c4aab14
    Malloc Post Memory
    Memory Addr w/ Ecache
    Load Post In Memory
    Run POST from MEM
    .........
loaded POST in memory
    Map PROM/STACK/NVRAM in DMMU
    Update Master Stack/Frame Pointers
All FPU Basic Tests
    FPU Regs Test
    FPU Move Regs Test
UPA Data Bus Line Test
Memory Tests
    Init Memory
    INFO:    256MB at bank 0 stack 0 (2 dimms per bank)
.............................................................
.............................................................
.............................................................
.....................................................
    INFO:      0MB at bank 0 stack 1
    INFO:      0MB at bank 2 stack 0
    INFO:      0MB at bank 2 stack 1
    ECC Memory Addr Test
    INFO:    256MB at bank 0 stack 0 (2 dimms per bank)
    INFO:      0MB at bank 0 stack 1
    INFO:      0MB at bank 2 stack 0
    INFO:      0MB at bank 2 stack 1
All Basic Sabre MMU Tests
    Init Sabre
```